REMARKS

Claims 1-46 are currently pending in the application. Claims 1-33 and 35-46 were finally rejected. Claim 34 was objected to.

The Examiner maintained and made final his rejection of claims 1-33 and 35-46 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0049824 A1 (Wilson). The rejection is respectfully traversed.

The Applicant thanks the Examiner for the courtesy of the phone conversation of October 24, 2005, during which the foregoing rejection was discussed. The Applicant also refers to and incorporates by reference the arguments set forth in the previous response to filed on September 12, 2005.

Wilson describes a multi-processor computer architecture having a distributed shared memory. The system includes a plurality of uniform memory access (UMA) cells 100 interconnected by an interconnect 20. Each UMA cell includes a processor 102 and a memory 104 which includes a memory controller 106. Each memory controller 106 includes a so-called "cache of history counter" (CofHC) 108. Each entry in CofHC 108 represents a page (indicated by page address field 112) in the associated memory 104 and includes a plurality of counters (e.g., 114-120 of Fig. 2). Each counter for a given entry tracks a different metric for the corresponding memory page. For example, each of counters 114, 115, and 116 corresponds to one of the other UMA's (e.g., 200, 300, etc.) in the system, and tracks the number of times the processor in the corresponding UMA accesses the memory page represented by that entry. Migration counter 118 is incremented upon each migration of the page, e.g., from one cache to another. Write counter 120 is incremented for each write to the page. By tracking these metrics, the system can determine (i.e., using the decision tree 250 of Fig. 3) whether there is a more efficient memory location for a given page in memory. See paragraphs [0023]-[0030].

Significantly, none of the counters described by Wilson determines or tracks transaction

latency. That is, as described above, Wilson tracks how many times a cached memory page is accessed by specific processors in the system so that it can then determine whether the page should be moved or copied to another cache. There is nothing which tracks latency, i.e., the time between two events, for individual system transactions, e.g., memory or I/O accesses.

By contrast, claim 1 of the present invention recites "a latency counter operable to generate a latency count for each of selected" memory transactions. That is, the recited latency counter maintains a count which is representative of the length of time (e.g., as measured in clock cycles) required to complete all or a portion of a particular memory or I/O transaction.

Claim 1 also recites "a plurality of histogram counters," each of which is "operable to count selected ones of the latency counts corresponding to an associated latency range." That is, each histogram counter tracks the number of transaction latencies (as determined by the latency counter) which fall within a particular latency range, e.g., 400 to 600 clock cycles. So, not only does the invention recited in claim 1 include the tracking of latencies for specific memory transactions, it also includes a second level of counting of the latency counts, i.e., where each of these transaction latencies fits with respect to multiple ranges within an overall time window.

An exemplary implementation is described in the present application from page 32, line 7 to page 33, line 21, with reference to Fig. 14. When a memory or I/O transaction begins, the Transaction Start signal is asserted, and when the transaction ends, the Transaction End signal is asserted. Between these two events, a latency counter counts the number of clock cycles. This maps to the latency counter and the latency count recited in claim 1. The resulting latency count is then placed in a "bucket" which corresponds to a latency range which includes that latency count, i.e., a histogram counter corresponding to the latency range is incremented. These "buckets" map to the histogram counter recited in claim 1. The present invention thus allows detailed latency data, e.g., a distribution of transaction latencies, to be accumulated during system operation.

Wilson neither describes nor suggests the determination or tracking of any type of latency as recited in claim 1 of the present application. Wilson does note that the information collected by the CoHC counters may be used to determine whether a particular memory page should be replicated or migrated to a different memory location which, in turn, may result in improvements in system latency (see paragraph [0030]). However, Wilson does not discuss how or even whether such latency improvements are determined. In fact, the present invention may be used with the technique of Wilson to determine whether Wilson's technique resulted in any improvement in system performance. In any case, latency measurements are clearly not performed or tracked using the CoHC counters or any of the other components of Wilson's system.

And because Wilson does not teach or suggest the tracking of individual transaction latencies, it also does not teach or suggest the tracking of how many such transaction latencies correspond to particular latency ranges. That is, Wilson also fails to show the use of histogram counters to count the latency counts as recited in claim 1.

Because Wilson fails to teach or suggest a latency counter which is operable to generate latency counts for transactions involving memory, and because Wilson also fails to teach or suggest a plurality of histogram counters for counting the latency counts for corresponding latency ranges, claim 1 is allowable over the Wilson reference for at least these reasons. And for similar reasons, claims 22, 38, and 41 are also believed to be allowable. In addition, all of the claims dependent on claims 1, 22, 38, and 41 are believed to be allowable for at least the reasons discussed.

The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter in claim 34. However, in view of the foregoing, claim 34 is believed to be allowable without amendment.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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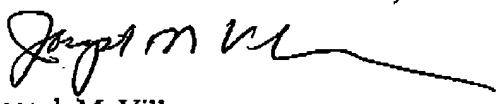

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